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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,484	04/08/2004	Michael G. Kelly	10031133-1	7400

57299 7590 05/21/2010

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
05/21/2010	ELECTRONIC

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL G. KELLY

Appeal 2009-002566
Application 10/820,484
Technology Center 2800

Decided: May 19, 2010

Before KENNETH W. HAIRSTON, THOMAS S. HAHN, and BRADLEY W. BAUMEISTER, *Administrative Patent Judges*.

BAUMEISTER, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-21. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

Appellant's invention relates to a semiconductor die that includes various metallizations that are disposed on the die's top and bottom surfaces for conducting either heat or electrical signals (Br. 2). Independent claim 1 is illustrative, reading as follows:

> 1: An integrated circuit system, comprising:
>
> a die incorporating an integrated circuit and having a top side and a bottom side, the top side supporting an electrical signal communication metallization and a top side thermal dissipation metallization, and the bottom side supporting a bottom side thermal dissipation metallization.

1. Claims 1-9 and 21 stand rejected under 35 U.S.C. § 103(a) as obvious over Hideshima (US 5,143,865) in view of Wu (US 2003/0067057 A1).

2. Claims 1-4 and 6-11 stand rejected under 35 U.S.C. § 103(a) as obvious over Hideshima in view of Kunikiyo (US 6,717,267 B1).

3. Claims 12 and 13 stand rejected under 35 U.S.C. § 103(a) as obvious over Hideshima in view of Kunikiyo and Wang (US 5,977,626).

4. Claim 14 stands rejected under 35 U.S.C. § 103(a) as obvious over Hideshima in view of Kunikiyo and Khan (US 6,853,070 B2).

5. Claims 15-18 stand rejected under 35 U.S.C. § 103(a) as obvious over Hideshima in view of White (US 5,665,655) and Kunikiyo.

6. Claims 19 and 20 stand rejected under 35 U.S.C. § 103(a) as obvious over Hideshima in view of White, Kunikiyo and Wang.

Hideshima is the primary reference for the two obviousness rejections of independent claim 1 (Ans. 3, 5). Hideshima's semiconductor device is a high power bipolar junction transistor module – a vertical transistor formed of a semiconductor chip that measures up to 10 mm x 10 mm (Hideshima, col. 4, ll. 62-68; Fig. 2). The semiconductor chip's substrate 11 includes a collector region, a well 12 formed within the top surface of the substrate and serving as the base region, and a plurality of emitter regions 13 formed within the surface of the base region (*id.* at Fig. 2). A nickel ohmic contact 16 and a solder layer 18C are formed on the bottom (collector) side of the chip (*id.* at col. 5, ll. 23-26; col. 6, ll. 18-20; Fig 2). A patterned aluminum wiring layer is formed on the top side of chip to serve as (1) a base electrode 15B for the solder bump 18B/43B; and (2) an emitter electrode 15E that interconnects the multiple emitter regions 13 and an overlying emitter solder bump 18E/43E (*id.* at col. 4, l. 62 – col. 5, l. 62; Figs. 2 and 7).

The Examiner's position is that (1) Hideshima's collector contact 16 and solder layer 43C correspond to the "bottom side thermal dissipation metallization" of claim 1; (2) the patterned wiring layer 15B/E corresponds to the "electrical signal communication metallization" on the top side of the chip; but (3) that Hideshima does not disclose the chip as further having a "top side thermal dissipation metallization" (Ans. 3). The Examiner finds that Wu provides motivation to attach Wu's lead frame die pad to the top surface of Hideshima's module "to allow the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package" (Ans. 4 (referencing Wu's Fig 3A embodiment wherein the central portion

of the chip surface on which electrical pads are also formed, is flip mounted onto a lead frame die pad)).

The Examiner also finds that Kunikiyo's dummy plug 31, which interconnects dummy interconnections to heat sink 32 (see Kunikiyo, col. 23, ll. 1-25; Fig. 19), could alternatively be incorporated into the top surface of Hideshima's module "to improve the circuit operation since the heat can be satisfactorily removed form [sic: from] the interlayer insulating films" (Ans. 5-6).

ISSUE

The issue before us, then, is: Does reasonable motivation exist to incorporate either of Wu's or Kunikiyo's thermal dissipation structures onto the top side of Hideshima's power transistor module?

ANALYSIS

I.

Appellant argues in relation to the combination of Hideshima and Wu, *inter alia*:

> The Examiner's position is that one skilled in the art would have been motivated to attach the die pad 21 disclosed in Wu to the top side of the semiconductor chip 10 disclosed in Hideshima et al. As explained above, however, the die pad 21 and the leads 222 are integral components of the lead frame (see, e.g., FIG. 2B of Wu). Therefore, it would not be possible to simply attach the die pad 21 of Wu to the central portion of the top side of the semiconductor chip 10 of Hideshima et al. without the other portions of the lead frame. As shown in FIG. 4 of Hideshima et al., however, such a modification would short-circuit the emitter regions 13 and the collector electrode 16 in Hideshima et al.'s semiconductor chip (see, e.g., FIG. 8). The fact is that

> the semiconductor chips disclosed in Hideshima et al. and Wu have different electrical connection needs. As a result, one skilled in the art would have to modify of the teachings of both references in ways that neither reference teaches or suggests in order to arrive at the inventive integrated circuit system as it is defined in claim 1.

(Br. 7-8).

Appellant's argument is persuasive. The discussion associated with Figures 4 and 5 of Hideshima indicates that, even assuming *arguendo* a die pad were able to be positioned on the top surface of the chip 10 without causing unwanted electrical short-circuiting, the die pad would not be thick enough to protrude from the surface of Hideshima's resin 33. As such, the inclusion of a die pad would not serve the function proposed by the Examiner – to conduct heat from the chip to ambient.

Furthermore, the configuration of copper metal plates 28-30, which serve as electrical contacts for the chip's collector, base, and emitter, respectively, indicate that the completed module is to be plugged into a receptacle with the top surface of the chip facing the receptacle (*see* Hideshima, Figs. 4-5). As such, any die pad disposed on this surface would not be exposed to the ambient environment, and as such, would be inhibited from conducting heat to ambient.

Accordingly, we find no reasonable motivation to incorporate Wu's die pad structure onto the top side of Hideshima's power transistor module. We therefore do not sustain the Examiner's rejection of the claims that were rejected as obvious over Hideshima in view of Wu, i.e., independent claim 1, and dependent claims 2-9 and 21, which depend from claim 1.

II.

Appellant similarly argues in relation to the combination of Hideshima and Kunikiyo, *inter alia*:

> The Examiner's position is that one skilled in the art would have been motivated to incorporate Kunikiyo's plugs 31 in the insulating film 17 on the top side of Hideshima et al.'s semiconductor chip 10. As explained above, however, the dummy plugs 31 only serve to connect the underlying dummy interconnections to the heat sink 32, which covers the entire top surface of Kunikiyo's semiconductor device, as shown in FIG. 19. It would not be possible to attach a heat sink of the type disclosed in Kunikiyo on the top side of Hideshima et al.'s semiconductor chip 10 because, as shown in FIG. 4 of Hideshima et al., such a modification would interfere with the interconnection between the lead frame and the solder bumps on the top surface of Hideshima et al.'s semiconductor chip 10. (See Hideshima et al., FIG. 8). The semiconductor chips disclosed in Hideshima et al. and Kunikiyo have different electrical connection needs. As a result, one skilled in the art would have had to modify of the teachings of both references in a way that neither reference teaches or suggests and that would not have been within the general knowledge of one of ordinary skill in the art in order to arrive at the inventive integrated circuit system as it is defined in claim 1.

(Br. 12).

Appellant's argument is persuasive. Kunikiyo's dummy plug is employed to thermally couple heat from the chip to a finned, external heat sink 32. But one of ordinary skill would not be motivated to include such a heat sink on the top surface of Hideshima's device because the heat sink would interfere with the electrical contact scheme disclosed by Hideshima, and it would interfere with plugging the power module into a receptacle.

Accordingly, Appellant has persuaded us that reasonable motivation did not exist to incorporate Kunikiyo's thermal plug onto the top side of Hideshima's power transistor module. We therefore do not sustain the Examiner's rejection of the claims that were rejected as obvious over Hideshima in view of Kunikiyo, i.e., independent claim 1, and dependent claims 2-4 and 6-11, which depend from claim 1.

III.

With respect to the remaining rejections of dependent claims 12-20, none of Wang, Khan, or White cures the deficiencies of the obviousness rejections explained above. For example, Wang discloses an integrated circuit system comprising: a die (22) incorporating an integrated circuit and having a top side (adjacent metal heat spreader 32) and a bottom side (adjacent substrate 20), the top side supporting an electrical signal communication metallization (the bond pads for wire bonds 26) and a top side thermal dissipation material (unlabeled material adjacent metal heat spreader supporting member 32c), and the bottom side supporting a bottom side thermal dissipation material (die attach material 24) (*see* e.g., col. 2, l. 10 – col. 4, l. 29; Fig. 2). However, Wang merely discloses that the thermal dissipation material provided on the top and bottom surfaces may be a die attach epoxy (col. 3, ll. 4-7; col. 4, ll. 2-4). The record contains no evidence either (1) that a metal film (or "metallization" as recited in claim 1) and die attach epoxy were art recognized functionally equivalent compositions; or (2) that it would have been otherwise obvious to substitute a metal film for the die attach epoxy. Accordingly, we do not sustain the rejections of claims 12-20 for the reasons discussed above.

DECISION

We reverse the Examiner's decision rejecting claims 1-21.

ORDER

REVERSED

Tkl

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